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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
MAZZONI ET AL.

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **A DEVICE FOR SENDING/RECEIVING DIGITAL DATA CAPABLE OF PROCESSING DIFFERENT BIT RATES, IN PARTICULAR IN A VDSL ENVIRONMENT**

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EXPRESS MAIL NO.: EL 768138046 US
DATE OF DEPOSIT: March 18, 2002
NAME: DAWN KIMLER
SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 3.

Please add new Claims 4 to 24.

4. A device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates, the device comprising:

a channel coding/decoding stage comprising

an interleaver,

a deinterleaver, and

a memory having a minimum size based upon a maximum bit rate of the group of predetermined bit rates and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device.

5. The device according to Claim 4 wherein said channel coding/decoding stage further comprises a Reed-Solomon coder/decoder connected to said interleaver and said deinterleaver and having a length N.

6. The device according to Claim 5 wherein said interleaver provides convolutional interleaving of I branches with i - 1 blocks of M bytes, and the deinterleaver provides convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

7. The device according to Claim 6 wherein the size of the first memory space is equal to $I \times (I - 1) \times M/2$ bytes, the size of the second memory space is equal to $I' \times (I' - 1) \times M'/2$ bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

8. The device according to Claim 6 wherein said interleaver and said deinterleaver respectively comprise a first addressing device and a second addressing device, said first and second addressing devices each comprising:

a first counter defining the relative index i or i' of a branch and having a counting limit value;

a second counter defining a number of bytes in a block and incremented each time that said first counter reaches its counting limit value;

a third counter defining the current index of a block in the branch with index i or i' to be incremented each time the block in the branch with index i or i' has M or M' bytes; and

an intermediate calculation device for calculating the address of each branch in said memory from the content of said first counter.

9. The device according to Claim 8 wherein said first addressing device further comprises a first address determination device for determining successive read and write addresses in said memory of data successively delivered to said interleaver and said first address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, and the parameter M.

10. The device according to Claim 8 wherein said second addressing device further comprises a second address determination device for determining successive read and write addresses in said memory of data successively delivered to said deinterleaver and said second address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, the parameter M', and the size of the first memory space.

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11. The device according to Claim 4 wherein said memory comprises a random access memory.

12. The device according to Claim 4 wherein said memory comprises a dual-port memory.

13. A device for sending and receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates, the device comprising:

a channel coding/decoding stage comprising

and interleaver,

a deinterleaver,

a random access memory whose minimum size is fixed as a function of a maximum bit rate of the group of predetermined bits and having a first memory space assigned to said interleaver and a second memory space assigned to said deinterleaver, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device, and

a Reed-Solomon coder/decoder connected to said interleaver and said deinterleaver and having a length N.

14. The device according to Claim 13 wherein said interleaver provides convolutional interleaving of I branches with i - 1 blocks of M bytes, and the deinterleaver provides convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

15. The device according to Claim 14 wherein the size of the first memory space is equal to $I \times (I - 1) \times M/2$ bytes, the size of the second memory space is equal to $I' \times (I' - 1) \times M'/2$ bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

16. The device according to Claim 14 wherein said interleaver and said deinterleaver respectively comprise a first addressing device and a second addressing device, said first and second addressing devices each comprising:

a first counter defining the relative index i or i' of a branch and having a counting limit value;

a second counter defining a number of bytes in a block and incremented each time that said first counter reaches its counting limit value;

a third counter defining the current index of a block in the branch with index i or i' to be incremented each time the block in the branch with index i or i' has M or M' bytes; and

an intermediate calculation device for calculating the address of each branch in said random access memory from the content of said first counter.

17. The device according to Claim 16 wherein said first addressing device further comprises a first address determination device for determining successive read and write addresses in said random access memory of data successively delivered to said interleaver and said first address determination device, the successive read and write addresses being determined based upon values supplied by said

intermediate calculation device, said second and third counters, and the parameter M.

18. The device according to Claim 16 wherein said second addressing device further comprises a second address determination device for determining successive read and write addresses in said random access memory of data successively delivered to said deinterleaver and said second address determination device, the successive read and write addresses being determined based upon values supplied by said intermediate calculation device, said second and third counters, the parameter M', and the size of the first memory space.

19. The device according to Claim 13 wherein said random access memory comprises a dual-port memory.

20. A method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising:

interleaving and deinterleaving the digital data;

setting a minimum size of a memory based upon a maximum bit rate of the group of predetermined bit rates; and

assigning a first memory space of the memory for interleaving and a second memory space of the memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device.

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21. The method according to Claim 20 further comprising performing Reed-Solomon coding and decoding for a length N of the digital data.

22. The method according to Claim 21 wherein interleaving comprises providing convolutional interleaving of I branches with i - 1 blocks of M bytes, and deinterleaving comprises providing convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, I and I' being sub-multiples of N and i and i' being current relative indexes of the branches.

23. The method according to Claim 22 wherein the size of the first memory space is equal to I × (I - 1) × M/2 bytes, the size of the second memory space is equal to I' × (I' - 1) × M'/2 bytes, and the sizes of the first and second memory spaces are set by I, I', M and M'.

24. The method according to Claim 20 wherein the memory comprises a random access memory.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

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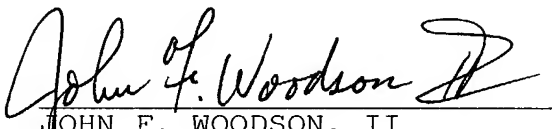
Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,



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A DEVICE FOR SENDING/RECEIVING DIGITAL DATA CAPABLE OF PROCESSING DIFFERENT BIT RATES, IN PARTICULAR IN A VDSL ENVIRONMENT

Field of the Invention

The present invention relates to the field of telecommunications, and, more particularly, to transmitters and receivers for data communication lines. Moreover, the invention relates ~~generally~~ to sending and receiving digital data that can have different bit rates, and ~~more particularly~~ to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates.

Background of the Invention

The present invention ~~is~~may advantageously be applied to a ~~VDSL (Very High Rate Digital Subscriber Line~~very high rate digital subscriber line (VDSL) environment or system, ~~i.e.~~for example, though the invention may also be used in other applications. That is, the invention applies to a digital communication system linking an operator and users via very high bit rate transmission lines. ~~This application is not limiting on the invention.~~

Thus, the invention applies more particularly to send/receive devices, usually referred to as "modems", at the operator and user ends of a transmission line. ~~The~~

Those skilled ~~person knows~~in the art will appreciate that a VDSL communication system is capable of delivering "symmetrical" services and "asymmetrical" services. A service is ~~referred to as "~~symmetrical" if the bit rate of information exchanged between the operator and the user in both transmission directions (i.e., from the operator to the user and from the user to the operator) is exactly the same.

A service is ~~referred to as "~~asymmetrical" if the bit rate of information sent in one transmission direction is different from the bit rate of information sent in the other transmission direction.

The processes of interleaving and deinterleaving data sent and received by a modem necessitates the use of memories. For a modem intended to operate at a predetermined bit rate, the memories must have a capacity that depends on that bit rate. ~~The~~

Summary of the Invention

An object of the invention ~~aims~~is to ~~propose~~provide a send/receive device (i.e., modem) architecture which requires a reduced quantity of memory~~,~~.

Yet another object of the invention is to provide such an architecture which can be used at the operator end or at the user end of a transmission line (~~in other words~~i.e., which is fully interchangeable between sending and receiving) ~~and~~.

Still another object of the invention is to provide such an architecture which is adaptable, ~~in particular~~particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates.

~~The invention therefore proposes in particular to use~~

These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send + receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).

The invention therefore ~~proposes~~provides a device for sending/receiving digital data ~~and~~that is capable of processing different bit rates from a group of predetermined bit rates (~~for example~~e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).

The device according to the invention ~~includes~~may include a coding/decoding stage (generally referred to by ~~the~~those skilled ~~person~~in the art as ~~"channel~~a "channel coding/decoding ~~stage"~~stage") including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of ~~said~~the group of predetermined bit rates (~~for example~~e.g., the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means. The size of each of the two

memory spaces is ~~parameterable~~set as a function of the bit rate actually processed by the device.

__In the context of the present invention, the term "bit rate" as associated with a memory capacity or memory space is ~~to be understood as being~~ a global bit rate, i.e.,_ the sum of the send and receive bit rates.

It is therefore possible to ~~reduce~~ considerably reduce the size of the memory means required for the interleaving and deinterleaving means implemented within a modem ~~that can~~. The modem may be used either at the operator end or at the user end, and ~~which~~it is capable of processing a number of different and symmetrical or asymmetrical bit rates.

The transmitted data stream ~~is generally~~may be protected from transmission channel noise by a Reed-Solomon coding algorithm, which is well known ~~to~~in the ~~skilled person~~art. To make the Reed-Solomon coding more efficient, the coding means ~~are~~may be coupled to the interleaving means ~~so as~~ to distribute in time errors introduced by the transmission channel~~, which~~. These errors often occur in bursts ~~affecting~~and affect several successive bytes, which can reduce the correction capacity of the Reed-Solomon code in isolation (generally eight bytes per packet). The interleaving means may then interleave the bytes temporally by modifying the order in which they are transmitted, which achieves ~~said~~the temporal distribution of the errors.

~~To be more precise, in one embodiment of the invention~~

More specifically, the channel coding/decoding stage ~~includes~~may include Reed-Solomon coding/decoding means of length N (where N = 240 bytes, for example).__ The interleaving means are then adapted

to effect convolutional interleaving of I branches with ~~i - 1~~i - 1 blocks of M bytes. The deinterleaving means are adapted to implement convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes. I and I' are sub-multiples of N, and i and i' are the current relative indexes of the branches. The size in bytes of the first memory space is equal to I × (I - 1) × M/2, and the size in bytes of the second memory space is equal to I' × (I' - 1) × M'/2. The sizes of the two memory spaces are ~~parameterable~~set by I, I', M and M'.

Using convolutional triangular interleaving (and, consequently, convolutional triangular deinterleaving), instead of ~~some~~ other conventional ~~type~~types of interleaving, is particularly beneficial because it reduces latency generated by the memory. Convolutional triangular interleaving requires a much smaller memory, which reduces latency. Latency is a primordial and decisive criterion for any VDSL communication system.

~~In one particularly simple embodiment of the invention the~~

The memory ~~is~~may be a random access memory, ~~in particular~~such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respectively include first addressing means and second addressing means. The first and second addressing means may each include:

a first counter defining the relative index i or i' of a branch,

and a second counter defining the number of bytes in a block and incremented each time that the first counter reaches its counting limit value. Moreover,

the first and second addressing means may also include a third counter defining the current index of a block in the branch with index i or i' and incremented each time that a block contains M or M' bytes, and

_intermediate calculation means calculating the address of each branch in ~~said~~the memory from the content of the first counter.

The first addressing means may further include first address determination means adapted to determine successive read and write addresses in ~~said~~the memory of data successively delivered to the interleaving means. _The first address determination means determine ~~said~~the addresses from values supplied by the intermediate calculation means, the second and third counters and the parameter M.

The second addressing means may further include second address determination means adapted to determine successive read and write addresses in ~~said~~the memory of data successively delivered to the deinterleaving means. _The second address determination means determine ~~said~~the addresses from values supplied by the intermediate calculation means, the second and third counters, the parameter M', and the size of the first memory space~~(~~. This is so that the first unoccupied address in the memory can be determined~~)~~.

Brief Description of the Drawings

Other advantages and features of the invention will become apparent ~~on~~upon examining the following detailed description of non-limiting embodiments of the invention and the accompanying drawings, in which:

~~- figure~~

FIG. 1 is a ~~highly diagrammatic representation~~schematic block diagram of a communication system in accordance with the invention linking two send/receive devices;

~~- figure~~

FIG. 2 ~~shows diagrammatically and in~~is a more ~~detail~~detailed schematic block diagram showing the internal architecture of a send/receive device according to the invention;

~~- figure~~

FIG. 3 ~~shows diagrammatically and in more detail~~is a schematic block diagram of the internal architecture of a coding/decoding stage of the device shown in ~~figure~~FIG. 2;

~~- figures~~

FIGS. 4 and 5 ~~show diagrammatically~~are schematic diagrams showing the theory of convolutional triangular interleaving and deinterleaving~~,~~ ~~- figure~~ of the present invention;

FIG. 6 ~~shows diagrammatically and in more detail~~is a schematic block diagram of the internal architecture of the interleaving and deinterleaving means of a send/receive device according to the invention;

~~- figure~~

FIG. 7 ~~shows diagrammatically one~~is a schematic block diagram of an embodiment of first addressing means associated with the interleaving means; and

~~- figure~~

FIG. 8 ~~shows diagrammatically one~~is a schematic block diagram of an embodiment of the second

addressing means associated with the deinterleaving means.

Detailed Description of the Preferred Embodiments

An application of the invention to a VDSL communication system will now be described, although the invention is not limited to ~~that~~this application. ~~Thus figure~~ Referring to FIG. 1 ~~shows,~~ two send/receive devices TO and TU according to the invention are shown, which may be referred to more simply as terminals or modems. One of these terminals, ~~for example~~e.g., the terminal TO, is at the operator end~~, and the~~. The other terminal TU is at the user end. The two modems are linked by a very high bit rate communication line LH.

The VDSL communication system enables the operator to provide symmetrical services, typically six symmetrical services S1-S6~~, i.e. services in which~~. That is, the information bit rates in the two transmission directions (i.e., from the operator to the user and from the user to the operator) are exactly the same. The service S1 with the lowest bit rate has a bit rate of 32 × 64 kbit/s, for example, and the fastest symmetrical service S6 has a bit rate of 362 × 64 kbit/s.

With the VDSL system, the operator can also provide "asymmetrical" services A1 - A6~~, i.e.~~. These are services with different information bit rates in the user to operator direction (uplink direction) and in the operator to user direction (downlink direction). The first asymmetrical service A1 has a bit rate in the uplink direction of 32 × 64 kbit/s, for example,

and a bit rate in the downlink direction of 100 × 64 kbit/s.

The asymmetrical service having the highest global information bit rate (uplink bit rate + downlink bit rate) is the service A6~~, whose~~. The bit rate of the service A6 in the uplink direction is equal to 32 × 64 kbit/s and ~~whose bit rate~~ in the downlink direction is equal to 832 × 64 kbit/s.

The send/receive device according to the invention can therefore be installed at the user end or at the operator end and is capable of processing all the above services, as described in more detail hereinafter~~, subject to choosing~~. Even so, the capacity of the memory assigned to the interleaving/deinterleaving means may need to be chosen in accordance with the maximum bit rate of the services offered, here the bit rate of the highest asymmetrical service (service A6)~~, and provided that~~. Furthermore, the parameters of the memory space of that memory ~~are~~may need to be set in accordance with the service actually processed by the device.

The internal architecture of the operator terminal TO from ~~figure~~FIG. 1 will now be described in more detail~~, and it is to~~. It should be understood that everything described hereinafter with respect to the operator terminal TO is equally valid for the terminal TU.

The terminal TO includes a send system and a receive system both connected to the transmission line LH ~~(see figure~~, as shown in FIG. 2~~)~~.

The terminal TO includes a channel coding/decoding stage ETC including a channel coding unit CC in the

send system and a channel decoding unit DCC in the receive system.

The channel coding unit CC includes Reed-Solomon coding means whose structure and function are ~~well~~ known to ~~the skilled person~~those of skill in the art. The Reed-Solomon coding means are associated with the interleaving means.

__In conjunction with subsequent interleaving, the Reed-Solomon coding can correct bursts of errors introduced by the transmission channel. Reed-Solomon coding is applied individually to each of the data packets delivered to the input of the coding unit CC.—

Reed-Solomon coding adds a number of parity bytes to the bytes of the packets received and can therefore correct a number of erroneous bytes. It is assumed here, by way of example, that the Reed-Solomon code used is an RS (240, 224) code with a correcting power of 8. This notation means that the Reed-Solomon coding means are applied to packets of 224 bytes, to which they add 16 parity bytes, to form a Reed-Solomon coded word whose length is 240 bytes~~,~~. ~~which~~This makes it possible to correct up to eight erroneous bytes. ~~In order to distribute temporally errors~~

Errors introduced by the channel, which often occur in bursts affecting several successive bytes and can therefore exceed the correction capacity of the Reed-Solomon code in isolation, may be distributed temporally. To do so, the bytes are temporally interleaved by modifying the order in which they are transmitted. _This improves the efficacy of the Reed-Solomon coding.

The information delivered to the output of the channel coding stage ETC is delivered to a modulation unit BM whose structure is known in the art and which effects quadrature modulation, for example. Then, after various standard processes have been effected in a send unit EM ~~including in particular,~~ which includes an interface to the transmission line LH, the modulated signal is transmitted over the transmission line LH.

Similarly, the receive system of the terminal TO includes at its input a receive unit ER including ~~in particular~~ a receive interface to the transmission line LH which effects standard processing. The modulated signal delivered to the output of the receive unit ER is demodulated in a demodulator unit BDM ~~and the~~. The demodulated signal is then delivered to the channel decoding unit DCC. The latter unit includes ~~in particular~~ deinterleaving and Reed-Solomon decoding means.

The internal architecture and the operation of the interleaving and deinterleaving means will now be described in more detail with more particular reference to ~~figures 3 et~~FIGS. 3-8. ~~seq.~~

As shown in ~~figure~~FIG. 3, and as already explained, the interleaving means MET follow the Reed-Solomon coding means CRS, and the deinterleaving means MDET precede the Reed-Solomon decoding means DCRS.

As shown diagrammatically in ~~figures~~FIGS. 4 and 5, the interleaving and deinterleaving are convolutional triangular interleaving and deinterleaving ~~with~~. There are I branches of ~~i - 1~~i - 1 blocks of M bytes for interleaving and I' branches of i' - 1 blocks of M' bytes for deinterleaving.

As explained in more detail hereinafter, the parameters I, M, I' and M' can be modified, ~~for example~~e.g., by software, and are delivered by control means MCD (~~figure~~see FIG. 3) ~~which can take the form of~~. The control means MCD may also be implemented in software. These parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means. This is done according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M').

The interleaving means therefore include I parallel branches BRi (numbered from 0 to I - 1, for example) which are implemented with a delay increment of M per branch (M represents the maximum number of bytes of a block BKj with index j). Each branch can be considered as a delay line, the length of the branch with index i~~, when~~ (where i varies in the range from 0 to I - 1~~,~~) being equal to ~~i ´ M~~i x M bytes. In ~~figure~~FIG. 4, by way of example, I = 7.

Accordingly, the first block of M bytes (having the index 0, for example) is not interleaved and is delivered unmodified to the output of the interleaving means. The next block of M bytes (index 1) is delivered to the input of the branch BR1, and so on up to the seventh block of M bytes (index 6), which is delivered to the branch BR6. The cycle then begins again with the blocks of bytes with indices from 7 to 13~~, the~~. The preceding blocks of bytes ~~being~~are either delivered to the output of the interleaving means or moved forward by one block BKj in the branch concerned.

The deinterleaving means associated with the interleaving means MET, and which are consequently incorporated into the user terminal TU, have a structure analogous to that which has just been described for the interleaving means. Yet, ~~but~~ the indices of the branches are reversed so that the longest interleaving time-delay corresponds to the shortest deinterleaving time-delay.

The deinterleaving means MDET incorporated in the operator terminal TO have I' branches, the branch with index i' having a length equal to i' × M' bytes.

For simplicity, ~~figure 5 represents~~ the situation in which I' = I is shown in FIG. 5. However, ~~but~~ if the service is an asymmetrical service, I and I' are generally different, of course, and likewise M and M'.

In hardware terms, as shown diagrammatically in ~~figure~~FIG. 6, the interleaving means and the deinterleaving means include common memory means MM, ~~for example~~e.g., a dual-port random access memory. The memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET.

The interleaving means also include first addressing means MAD1 receiving the parameters I and M ~~and the~~. The deinterleaving means also include second addressing means MAD2 receiving the parameters I' and M'. The structure of the addressing means is described in more detail hereinafter with reference to ~~figures~~FIGS. 7 and 8.

The minimum size of the memory MM is set by the maximum bit rate that the send/receive device can

process. The maximum bit rate is, of course, the sum of the uplink bit rate and the downlink bit rate.

In this example, the maximum bit rate is that of the largest asymmetrical service A6.

An example of the capacity of the memory MM and of the values chosen for the parameters I, M, I' and M' ~~follows~~ for an asymmetrical service A6 and an RS (240, 224) Reed-Solomon code with a correction power of 8 bytes/word~~,~~ may be as follows when the transmission lines are disturbed by an impulsive noise with a duration of 0.25 ms.

In the downlink direction, the maximum bit rate is equal to 832 × 64 kbit/s.

The number of bits affected by noise is consequently equal to the product of that bit rate by the duration of the impulsive noise, which yields a number of bits affected by noise equal to ~~13 312~~13,312 (~~1 664~~1,664 bytes). Given the correcting power of the Reed-Solomon code (here 8), the number nrs of Reed-Solomon words needed to correct ~~1 664~~1,664 bytes subject to noise is equal to ~~1 664/8~~1,664/8, i.e. 208.

The size of the memory space needed to store this maximum bit rate is then equal to N × nrs/2, where N is the size of the Reed-Solomon code (here 240).

The resulting memory space size is therefore equal to ~~24 960~~24,960 bytes.

The bit rate in the uplink direction is equal to 32 × 64 kbit/s. A similar calculation shows that the number of bits affected by noise is equal to 512, and that nrs = 8. The memory size to be provided for the uplink direction is therefore equal to ~~1 920~~1,920 bytes. The minimum size of the memory MM is therefore ~~26 880~~26,880 bytes.

The parameters I, I', M and M' can be determined from the above capacities. ~~To be more precise~~More particularly, the size of the first memory space needed to implement triangular convolutional interleaving with I branches of ~~i-1~~i-1 blocks of M bytes is equal to I × (I - 1) × M/2.

Similarly, the size of the second memory space ESM2 required to support the uplink bit rate is equal to I' × (I' - 1) × M'/2.

Also, I and I' must be sub-multiples of the size N of the Reed-Solomon code.

Since I × (I - 1) × M/2 must be equal to ~~24 960~~24,960, it is possible to choose I = 40 and M = 32. Similarly, because I' × (I' - 1) × M'/2 must be at least equal to ~~1 920~~1,920, it is possible to choose I' = 24 and M' = 7~~ (this~~. This requires a slight increase in size to ~~1 932~~1,932 to facilitate the implementation~~)~~.

The final size of the memory MM is therefore equal to 26 892 bytes.

The above calculation of I, M, I' and M' for the asymmetrical service A6 can be applied in an analogous manner to the other services of the VDSL system. A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage. When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD ~~fetch~~may retrieve the corresponding values of I, M, I' and M' from the stored table~~ and deliver them~~. These values are delivered to the addressing means MAD1 and MAD2, the

structure of which is described in more detail ~~next~~ with reference to ~~figures~~FIGS. 7 and 8.

~~Figure 7 shows that~~

As shown in FIG. 7, the first addressing means include a first counter CT1 delivering the relative index i of a branch BRi at the timing rate of a clock signal. The index i is delivered to intermediate calculation means MCI that determine the address adbs of the branch BRi in the first memory space. ~~To be more precise~~More specifically, the address adbs is equal to ~~i~~ i x (~~i~~i - 1)/2. The means MCI can be easily implemented using multipliers, dividers and subtractors.

The first counter CTI has a counting range equal to I and therefore counts from 0 to I - 1, for example.

The means MD1 further include a second counter CT2 which delivers a current value m equal to the current number of bytes in each block BKj of a branch BRi. The counting range of the counter CT2 is equal to M. In other words, m can vary from 0 to ~~M~~M - 1, for example.

The second counter CT2 is incremented by one unit each time that ~~i = I~~i = I - 1.

The means MDA1 further include a third counter CT3 which delivers the index j of the block BKj within the branch with index i. The counting range of the counter CT3 is equal to i. In other words, j varies from 0 to ~~i~~i - 1, for example. The third counter CT3 is incremented each time that a block contains M bytes, and therefore in this example each time that the counter CT2 reaches the value M.

The means MDA1 further include first address determination means MD1 which determine the read address ar in the memory and the write address aw in the memory.

~~To be more precise~~ More precisely, the read address ar is equal to (adbs + j) × M + m.

__The write address aw is then simply equal to the read address but delayed by one cycle of the clock signal.

__Again, the means MD1 can be easily implemented using adders and multipliers.

For example, a small auxiliary dual-port memory with a capacity of (I - 1) × M bits can be used to store the value of the index j delivered by the third counter CT3, which is incremented every M clock cycles. Every M clock cycles, the value of j corresponds to the ~~i-th~~ith branch in the auxiliary memory, after which the counter CT3 is incremented and the new value is rewritten at the same address.

The second addressing means MDA2 that deliver the read address ar' and the write address aw' in the second memory space of the memory MM have a structure similar to that just described for the first addressing means MDA1. Only the differences between the means MDA1 and the means MDA2 are described ~~here~~herein.

__The first counter CT10 delivers the relative index i' of a branch. This time i' varies in the range ~~from~~of I' - 1 to 0. The intermediate calculation means MCI deliver the address of each branch adbs' using a formula analogous to that used to calculate the address, but substituting i' for i.

The second counter CT20 defines the number m' of bytes in a block and is incremented each time that the counter CT10 reaches its counting limit value, in

this example when i' reaches the value 0. In this example, the second counter CT20 varies in the range from 0 to M' - 1.

The third counter CT30 defines the current index j' of a block in the branch with index i'. It varies in the range from 0 to i' - 1 and is incremented each time that a block contains M' bytes, i.e., when the second counter CT20 reaches the value M'.

The second addressing means MDA2 include second address determination means MD2 which determine the write address aw' and the read address ar'. However, the second address determination means MD2 must allow for the size OF of the first memory space ESM1, which is defined by equation (1) below:

$$OF = I \times (I - 1) \times M/2, \qquad (1)$$

and ~~is~~may be stored in a register, for example. For uplink interleaving, the addresses of the memory MM vary in the range ~~from~~of 0 to OF - 1.

The first unoccupied address in the memory MM therefore has the value OF.

The means MD2 then calculate the read address ar' from equation (2) below:

$$ar' = OF + \text{~~M' ·~~}M' \times (adbs' + j') + m' \qquad (2)$$

The write address aw' is equal to the read address and is available on the next clock pulse.

Of course, everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving

means with I' branches. For the user terminal TU it is then necessary to substitute I' for I, and vice versa, and M' for M, and vice versa, in ~~all of~~ the foregoing description.

__It would equally be possible to use a single-port memory in place of a dual-port memory by adopting a clock signal ~~of double~~having twice the frequency.

THAT WHICH IS CLAIMED IS:

1. A device for sending/receiving digital data and capable of processing different bit rates from a group of predetermined bit rates, said device including a channel coding/decoding stage including interleaving means (MET) and deinterleaving means (MDET) including a memory (MM) whose minimum size is fixed as a function of the maximum bit rate of said group and having a first memory space (ESM1) assigned to the interleaving means and a second memory space (ESM2) assigned to the deinterleaving means, the size of each of the two memory spaces being parameterable as a function of the bit rate actually processed by the device.

2. A device according to claim 1, characterized in that the channel coding/decoding stage includes Reed-Solomon coding/decoding means (CRS, DCRS) of length N, in that the interleaving means (MET) are adapted to effect convolutional interleaving of I branches with ~~i - 1~~i - 1 blocks of M bytes and the deinterleaving means are adapted to implement convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, I and I' being sub-multiples of N and i and i' being the current relative indexes of the branches, in that the size in bytes of the first memory space is equal to $I \times (I - 1) \times M/2$ and the size in bytes of the second memory space is equal to $I' \times (I' - 1) \times M'/2$, and in that the sizes of the two memory spaces are parameterable by I, I', M and M'.

3. A device according to claim 2, characterized in that the memory (MM) is a random

access memory, in particular a dual-port memory, the interleaving means and the deinterleaving means respectively include first addressing means (MDA1) and second addressing means (MDA2), said addressing means each include:

a first counter (CT1, CT10) defining the relative index i or i' of a branch,

a second counter (CT2, CT20) defining the number of bytes in a block and incremented each time that the first counter reaches its counting limit value,

a third counter (CT3, CT30) defining the current index of a block in the branch with index i or i' and incremented each time that a block contains M or M' bytes,

intermediate calculation means (MCI) calculating the address (adbs, adbs') of each branch in said memory from the content of the first counter,

the first addressing means (MDA1) further include first address determination means (MD1) adapted to determine successive read and write addresses in said memory of data successively delivered to the interleaving means and said first address determination means (MD1) determine said addresses from values supplied by the intermediate calculation means (MCI), the second and third counters (CT2, CT3) and the parameter M, and

the second addressing means (MDA2) further include second address determination means (MD2) adapted to determine successive read and write addresses in said memory of data successively delivered to the deinterleaving means and said second address determination means (MD2) determine said addresses from

values supplied by the intermediate calculation means (MCI), the second and third counters (CT20, CT30), the parameter M' and the size (OF) of the first memory space.

A DEVICE FOR SENDING/RECEIVING DIGITAL DATA CAPABLE OF PROCESSING DIFFERENT BIT RATES, IN PARTICULAR IN A VDSL ENVIRONMENT

Abstract of the Disclosure

A device for sending/receiving digital data is capable of processing different bit rates from a group of predetermined bit rates. ~~It includes~~ The device may include a channel coding/decoding stage including ~~interleaving means MET and deinterleaving means MDET including~~an interleaver, a deinterleaver, and a memory ~~MM~~ whose minimum size is fixed as a function of the maximum bit rate of ~~said~~the group ~~and having~~of predetermined bit rates. The memory may have a first memory space ~~ESM1~~ assigned to the ~~interleaving means~~interleaver and a second memory space ~~ESM2~~ assigned to the ~~deinterleaving means.~~deinterleaver. The size of each of the two memory spaces ~~is parameterable~~may be set as a function of the bit rate actually processed by the device.

~~Reference : figure 6.~~

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SUBSTITUTE SPECIFICATION

A DEVICE FOR SENDING/RECEIVING DIGITAL DATA CAPABLE OF PROCESSING DIFFERENT BIT RATES, IN PARTICULAR IN A VDSL ENVIRONMENT

Field of the Invention

The present invention relates to the field of telecommunications, and, more particularly, to transmitters and receivers for data communication lines. Moreover, the invention relates to sending and receiving digital data that can have different bit rates, and to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates.

Background of the Invention

The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications. That is, the invention applies to a digital communication system linking an operator and users via very high bit rate transmission lines. Thus, the invention applies more particularly to send/receive devices, usually referred to as modems, at the operator and user ends of a transmission line.

Those skilled in the art will appreciate that a VDSL communication system is capable of delivering symmetrical services and asymmetrical services. A service is symmetrical if the bit rate of information exchanged between the operator and the user in both transmission directions (i.e., from the operator to the user and from the user to the operator) is exactly the same. A service is asymmetrical if the bit rate of information sent in one transmission direction is different from the bit rate of information sent in the other transmission direction.

The processes of interleaving and deinterleaving data sent and received by a modem necessitates the use of memories. For a modem intended to operate at a predetermined bit rate, the memories must have a capacity that depends on that bit rate.

Summary of the Invention

An object of the invention is to provide a send/receive device (i.e., modem) architecture which requires a reduced quantity of memory.

Yet another object of the invention is to provide such an architecture which can be used at the operator end or at the user end of a transmission line (i.e., which is fully interchangeable between sending and receiving).

Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates.

These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send + receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem). The invention therefore provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).

The device according to the invention may include a coding/decoding stage (generally referred to by those skilled in the art as a "channel coding/decoding stage") including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means. The size of each of the two memory spaces is set as a function of the bit rate actually processed by the device. In the context of the present invention, the term "bit rate" as associated with a memory capacity or memory space is a global bit rate, i.e., the sum of the send and receive bit rates.

It is therefore possible to considerably reduce the size of the memory means required for the

interleaving and deinterleaving means implemented within a modem. The modem may be used either at the operator end or at the user end, and it is capable of processing a number of different and symmetrical or asymmetrical bit rates.

The transmitted data stream may be protected from transmission channel noise by a Reed-Solomon coding algorithm, which is well known in the art. To make the Reed-Solomon coding more efficient, the coding means may be coupled to the interleaving means to distribute in time errors introduced by the transmission channel. These errors often occur in bursts and affect several successive bytes, which can reduce the correction capacity of the Reed-Solomon code in isolation (generally eight bytes per packet). The interleaving means may then interleave the bytes temporally by modifying the order in which they are transmitted, which achieves the temporal distribution of the errors.

More specifically, the channel coding/decoding stage may include Reed-Solomon coding/decoding means of length N (where N = 240 bytes, for example). The interleaving means are then adapted to effect convolutional interleaving of I branches with i - 1 blocks of M bytes. The deinterleaving means are adapted to implement convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes. I and I' are sub-multiples of N, and i and i' are the current relative indexes of the branches. The size in bytes of the first memory space is equal to $I \times (I - 1) \times M/2$, and the size in bytes of the second memory space is

equal to I' × (I' - 1) × M'/2. The sizes of the two memory spaces are set by I, I', M and M'.

Using convolutional triangular interleaving (and, consequently, convolutional triangular deinterleaving) instead of other conventional types of interleaving is particularly beneficial because it reduces latency generated by the memory. Convolutional triangular interleaving requires a much smaller memory, which reduces latency. Latency is a primordial and decisive criterion for any VDSL communication system.

The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respectively include first addressing means and second addressing means. The first and second addressing means may each include a first counter defining the relative index i or i' of a branch, and a second counter defining the number of bytes in a block and incremented each time that the first counter reaches its counting limit value. Moreover, the first and second addressing means may also include a third counter defining the current index of a block in the branch with index i or i' and incremented each time that a block contains M or M' bytes, and intermediate calculation means calculating the address of each branch in the memory from the content of the first counter.

The first addressing means may further include first address determination means adapted to determine successive read and write addresses in the memory of data successively delivered to the interleaving means. The first address determination means determine the addresses from values supplied by

the intermediate calculation means, the second and third counters and the parameter M.

The second addressing means may further include second address determination means adapted to determine successive read and write addresses in the memory of data successively delivered to the deinterleaving means. The second address determination means determine the addresses from values supplied by the intermediate calculation means, the second and third counters, the parameter M', and the size of the first memory space. This is so that the first unoccupied address in the memory can be determined.

Brief Description of the Drawings

Other advantages and features of the invention will become apparent upon examining the following detailed description of non-limiting embodiments of the invention and the accompanying drawings, in which:

FIG. 1 is a schematic block diagram of a communication system in accordance with the invention linking two send/receive devices;

FIG. 2 is a more detailed schematic block diagram showing the internal architecture of a send/receive device according to the invention;

FIG. 3 is a schematic block diagram of the internal architecture of a coding/decoding stage of the device shown in FIG. 2;

FIGS. 4 and 5 are schematic diagrams showing the theory of convolutional triangular interleaving and deinterleaving of the present invention;

FIG. 6 is a schematic block diagram of the internal architecture of the interleaving and

deinterleaving means of a send/receive device according to the invention;

FIG. 7 is a schematic block diagram of an embodiment of first addressing means associated with the interleaving means; and

FIG. 8 is a schematic block diagram of an embodiment of the second addressing means associated with the deinterleaving means.

Detailed Description of the Preferred Embodiments

An application of the invention to a VDSL communication system will now be described, although the invention is not limited to this application. Referring to FIG. 1, two send/receive devices TO and TU according to the invention are shown, which may be referred to more simply as terminals or modems. One of these terminals, e.g., the terminal TO, is at the operator end. The other terminal TU is at the user end. The two modems are linked by a very high bit rate communication line LH.

The VDSL communication system enables the operator to provide symmetrical services, typically six symmetrical services S1-S6. That is, the information bit rates in the two transmission directions (i.e., from the operator to the user and from the user to the operator) are exactly the same. The service S1 with the lowest bit rate has a bit rate of 32 × 64 kbit/s, for example, and the fastest symmetrical service S6 has a bit rate of 362 × 64 kbit/s.

With the VDSL system, the operator can also provide asymmetrical services A1 - A6. These are services with different information bit rates in the

user to operator direction (uplink direction) and in the operator to user direction (downlink direction). The first asymmetrical service A1 has a bit rate in the uplink direction of 32 × 64 kbit/s, for example, and a bit rate in the downlink direction of 100 × 64 kbit/s. The asymmetrical service having the highest global information bit rate (uplink bit rate + downlink bit rate) is the service A6. The bit rate of the service A6 in the uplink direction is equal to 32 × 64 kbit/s and in the downlink direction is equal to 832 × 64 kbit/s.

The send/receive device according to the invention can therefore be installed at the user end or at the operator end and is capable of processing all the above services, as described in more detail hereinafter. Even so, the capacity of the memory assigned to the interleaving/deinterleaving means may need to be chosen in accordance with the maximum bit rate of the services offered, here the bit rate of the highest asymmetrical service (service A6). Furthermore, the parameters of the memory space of that memory may need to be set in accordance with the service actually processed by the device.

The internal architecture of the operator terminal TO from FIG. 1 will now be described in more detail. It should be understood that everything described hereinafter with respect to the operator terminal TO is equally valid for the terminal TU. The terminal TO includes a send system and a receive system both connected to the transmission line LH, as shown in FIG. 2. The terminal TO includes a channel coding/decoding stage ETC including a channel coding

unit CC in the send system and a channel decoding unit DCC in the receive system.

The channel coding unit CC includes Reed-Solomon coding means whose structure and function are known to those of skill in the art. The Reed-Solomon coding means are associated with the interleaving means. In conjunction with subsequent interleaving, the Reed-Solomon coding can correct bursts of errors introduced by the transmission channel. Reed-Solomon coding is applied individually to each of the data packets delivered to the input of the coding unit CC.

Reed-Solomon coding adds a number of parity bytes to the bytes of the packets received and can therefore correct a number of erroneous bytes. It is assumed here, by way of example, that the Reed-Solomon code used is an RS (240, 224) code with a correcting power of 8. This notation means that the Reed-Solomon coding means are applied to packets of 224 bytes, to which they add 16 parity bytes, to form a Reed-Solomon coded word whose length is 240 bytes. This makes it possible to correct up to eight erroneous bytes.

Errors introduced by the channel, which often occur in bursts affecting several successive bytes and can therefore exceed the correction capacity of the Reed-Solomon code in isolation, may be distributed temporally. To do so, the bytes are temporally interleaved by modifying the order in which they are transmitted. This improves the efficacy of the Reed-Solomon coding.

The information delivered to the output of the channel coding stage ETC is delivered to a modulation unit BM whose structure is known in the art and which effects quadrature modulation, for example.

Then, after various standard processes have been effected in a send unit EM, which includes an interface to the transmission line LH, the modulated signal is transmitted over the transmission line LH.

Similarly, the receive system of the terminal TO includes at its input a receive unit ER including a receive interface to the transmission line LH which effects standard processing. The modulated signal delivered to the output of the receive unit ER is demodulated in a demodulator unit BDM. The demodulated signal is then delivered to the channel decoding unit DCC. The latter unit includes deinterleaving and Reed-Solomon decoding means.

The internal architecture and the operation of the interleaving and deinterleaving means will now be described in more detail with more particular reference to FIGS. 3-8. As shown in FIG. 3, and as already explained, the interleaving means MET follow the Reed-Solomon coding means CRS, and the deinterleaving means MDET precede the Reed-Solomon decoding means DCRS. As shown diagrammatically in FIGS. 4 and 5, the interleaving and deinterleaving are convolutional triangular interleaving and deinterleaving. There are I branches of i - 1 blocks of M bytes for interleaving and I' branches of i' - 1 blocks of M' bytes for deinterleaving.

As explained in more detail hereinafter, the parameters I, M, I' and M' can be modified, e.g., by software, and are delivered by control means MCD (see FIG. 3). The control means MCD may also be implemented in software. These parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means. This is done

according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M').

The interleaving means therefore include I parallel branches BRi (numbered from 0 to I - 1, for example) which are implemented with a delay increment of M per branch (M represents the maximum number of bytes of a block BKj with index j). Each branch can be considered as a delay line, the length of the branch with index i (where i varies in the range from 0 to I - 1) being equal to i × M bytes. In FIG. 4, by way of example, I = 7.

Accordingly, the first block of M bytes (having the index 0, for example) is not interleaved and is delivered unmodified to the output of the interleaving means. The next block of M bytes (index 1) is delivered to the input of the branch BR1, and so on up to the seventh block of M bytes (index 6), which is delivered to the branch BR6. The cycle then begins again with the blocks of bytes with indices from 7 to 13. The preceding blocks of bytes are either delivered to the output of the interleaving means or moved forward by one block BKj in the branch concerned.

The deinterleaving means associated with the interleaving means MET, and which are consequently incorporated into the user terminal TU, have a structure analogous to that which has just been described for the interleaving means. Yet, the indices of the branches are reversed so that the longest interleaving time-delay corresponds to the shortest deinterleaving time-delay. The deinterleaving means MDET incorporated in the operator terminal TO have I'

branches, the branch with index i' having a length equal to i' × M' bytes.

For simplicity, the situation in which I' = I is shown in FIG. 5. However, if the service is an asymmetrical service, I and I' are generally different, of course, and likewise M and M'. In hardware terms, as shown diagrammatically in FIG. 6, the interleaving means and the deinterleaving means include common memory means MM, e.g., a dual-port random access memory. The memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET.

The interleaving means also include first addressing means MAD1 receiving the parameters I and M. The deinterleaving means also include second addressing means MAD2 receiving the parameters I' and M'. The structure of the addressing means is described in more detail hereinafter with reference to FIGS. 7 and 8. The minimum size of the memory MM is set by the maximum bit rate that the send/receive device can process. The maximum bit rate is, of course, the sum of the uplink bit rate and the downlink bit rate.

In this example, the maximum bit rate is that of the largest asymmetrical service A6. An example of the capacity of the memory MM and of the values chosen for the parameters I, M, I' and M' for an asymmetrical service A6 and an RS (240, 224) Reed-Solomon code with a correction power of 8 bytes/word may be as follows when the transmission lines are disturbed by an impulsive noise with a duration of 0.25 ms.

In the downlink direction, the maximum bit rate is equal to 832 × 64 kbit/s. The number of bits

affected by noise is consequently equal to the product of that bit rate by the duration of the impulsive noise, which yields a number of bits affected by noise equal to 13,312 (1,664 bytes). Given the correcting power of the Reed-Solomon code (here 8), the number nrs of Reed-Solomon words needed to correct 1,664 bytes subject to noise is equal to 1,664/8, i.e. 208. The size of the memory space needed to store this maximum bit rate is then equal to N×nrs/2, where N is the size of the Reed-Solomon code (here 240). The resulting memory space size is therefore equal to 24,960 bytes.

The bit rate in the uplink direction is equal to 32 × 64 kbit/s. A similar calculation shows that the number of bits affected by noise is equal to 512, and that nrs = 8. The memory size to be provided for the uplink direction is therefore equal to 1,920 bytes. The minimum size of the memory MM is therefore 26,880 bytes.

The parameters I, I', M and M' can be determined from the above capacities. More particularly, the size of the first memory space needed to implement triangular convolutional interleaving with I branches of i-1 blocks of M bytes is equal to $I \times (I - 1) \times M/2$. Similarly, the size of the second memory space ESM2 required to support the uplink bit rate is equal to $I' \times (I' - 1) \times M'/2$. Also, I and I' must be sub-multiples of the size N of the Reed-Solomon code.

Since $I \times (I - 1) \times M/2$ must be equal to 24,960, it is possible to choose I = 40 and M = 32. Similarly, because $I' \times (I' - 1) \times M'/2$ must be at least equal to 1,920, it is possible to choose I' = 24

and M' = 7. This requires a slight increase in size to 1,932 to facilitate the implementation. The final size of the memory MM is therefore equal to 26 892 bytes.

The above calculation of I, M, I' and M' for the asymmetrical service A6 can be applied in an analogous manner to the other services of the VDSL system. A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage. When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I' and M' from the stored table. These values are delivered to the addressing means MAD1 and MAD2, the structure of which is described in more detail with reference to FIGS. 7 and 8.

As shown in FIG. 7, the first addressing means include a first counter CT1 delivering the relative index i of a branch BRi at the timing rate of a clock signal. The index i is delivered to intermediate calculation means MCI that determine the address adbs of the branch BRi in the first memory space. More specifically, the address adbs is equal to $i \times (i - 1)/2$. The means MCI can be easily implemented using multipliers, dividers and subtractors.

The first counter CTI has a counting range equal to I and therefore counts from 0 to I - 1, for example. The means MD1 further include a second counter CT2 which delivers a current value $\underline{m}$ equal to the current number of bytes in each block BKj of a branch BRi. The counting range of the counter CT2 is equal to M. In other words, $\underline{m}$ can vary from 0 to M -

1, for example. The second counter CT2 is incremented by one unit each time that i = I - 1.

The means MDA1 further include a third counter CT3 which delivers the index j of the block BKj within the branch with index i. The counting range of the counter CT3 is equal to i. In other words, j varies from 0 to i - 1, for example. The third counter CT3 is incremented each time that a block contains M bytes, and therefore in this example each time that the counter CT2 reaches the value M.

The means MDA1 further include first address determination means MD1 which determine the read address ar in the memory and the write address aw in the memory. More precisely, the read address ar is equal to (adbs + j) × M + m. The write address aw is then simply equal to the read address but delayed by one cycle of the clock signal. Again, the means MD1 can be easily implemented using adders and multipliers.

For example, a small auxiliary dual-port memory with a capacity of (I - 1) × M bits can be used to store the value of the index j delivered by the third counter CT3, which is incremented every M clock cycles. Every M clock cycles, the value of j corresponds to the ith branch in the auxiliary memory, after which the counter CT3 is incremented and the new value is rewritten at the same address.

The second addressing means MDA2 that deliver the read address ar' and the write address aw' in the second memory space of the memory MM have a structure similar to that just described for the first addressing means MDA1. Only the differences between the means MDA1 and the means MDA2 are described herein. The first counter CT10 delivers the relative index i' of a

branch. This time i' varies in the range of I' - 1 to 0. The intermediate calculation means MCI deliver the address of each branch adbs' using a formula analogous to that used to calculate the address, but substituting i' for i.

The second counter CT20 defines the number m' of bytes in a block and is incremented each time that the counter CT10 reaches its counting limit value, in this example when i' reaches the value 0. In this example, the second counter CT20 varies in the range from 0 to M' - 1. The third counter CT30 defines the current index j' of a block in the branch with index i'. It varies in the range from 0 to i' - 1 and is incremented each time that a block contains M' bytes, i.e., when the second counter CT20 reaches the value M'.

The second addressing means MDA2 include second address determination means MD2 which determine the write address aw' and the read address ar'. However, the second address determination means MD2 must allow for the size OF of the first memory space ESM1, which is defined by equation (1) below:

$$OF = I \times (I - 1) \times M/2, \qquad (1)$$

and may be stored in a register, for example. For uplink interleaving, the addresses of the memory MM vary in the range of 0 to OF - 1.

The first unoccupied address in the memory MM therefore has the value OF. The means MD2 then calculate the read address ar' from equation (2) below:

$$ar' = OF + M' \times (adbs' + j') + m'. \qquad (2)$$

The write address aw' is equal to the read address and is available on the next clock pulse.

Of course, everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving means with I' branches. For the user terminal TU it is then necessary to substitute I' for I, and vice versa, and M' for M, and vice versa, in the foregoing description. It would equally be possible to use a single-port memory in place of a dual-port memory by adopting a clock signal having twice the frequency.

THAT WHICH IS CLAIMED IS:

1. A device for sending/receiving digital data and capable of processing different bit rates from a group of predetermined bit rates, said device including a channel coding/decoding stage including interleaving means (MET) and deinterleaving means (MDET) including a memory (MM) whose minimum size is fixed as a function of the maximum bit rate of said group and having a first memory space (ESM1) assigned to the interleaving means and a second memory space (ESM2) assigned to the deinterleaving means, the size of each of the two memory spaces being parameterable as a function of the bit rate actually processed by the device.

2. A device according to claim 1, characterized in that the channel coding/decoding stage includes Reed-Solomon coding/decoding means (CRS, DCRS) of length N, in that the interleaving means (MET) are adapted to effect convolutional interleaving of I branches with i - 1 blocks of M bytes and the deinterleaving means are adapted to implement convolutional deinterleaving with I' branches of i' - 1 blocks of M' bytes, I and I' being sub-multiples of N and i and i' being the current relative indexes of the branches, in that the size in bytes of the first memory space is equal to $I \times (I - 1) \times M/2$ and the size in bytes of the second memory space is equal to $I' \times (I' - 1) \times M'/2$, and in that the sizes of the two memory spaces are parameterable by I, I', M and M'.

3. A device according to claim 2, characterized in that the memory (MM) is a random access memory, in particular a dual-port memory, the interleaving means and the deinterleaving means respectively include first addressing means (MDA1) and second addressing means (MDA2), said addressing means each include:

a first counter (CT1, CT10) defining the relative index i or i' of a branch,

a second counter (CT2, CT20) defining the number of bytes in a block and incremented each time that the first counter reaches its counting limit value,

a third counter (CT3, CT30) defining the current index of a block in the branch with index i or i' and incremented each time that a block contains M or M' bytes,

intermediate calculation means (MCI) calculating the address (adbs, adbs') of each branch in said memory from the content of the first counter,

the first addressing means (MDA1) further include first address determination means (MD1) adapted to determine successive read and write addresses in said memory of data successively delivered to the interleaving means and said first address determination means (MD1) determine said addresses from values supplied by the intermediate calculation means (MCI), the second and third counters (CT2, CT3) and the parameter M, and

the second addressing means (MDA2) further include second address determination means (MD2) adapted to determine successive read and write addresses in said memory of data successively delivered

to the deinterleaving means and said second address determination means (MD2) determine said addresses from values supplied by the intermediate calculation means (MCI), the second and third counters (CT20, CT30), the parameter M' and the size (OF) of the first memory space.

A DEVICE FOR SENDING/RECEIVING DIGITAL DATA CAPABLE OF PROCESSING DIFFERENT BIT RATES, IN PARTICULAR IN A VDSL ENVIRONMENT

Abstract of the Disclosure

A device for sending/receiving digital data is capable of processing different bit rates from a group of predetermined bit rates. The device may include a channel coding/decoding stage including an interleaver, a deinterleaver, and a memory whose minimum size is fixed as a function of the maximum bit rate of the group of predetermined bit rates. The memory may have a first memory space assigned to the interleaver and a second memory space assigned to the deinterleaver. The size of each of the two memory spaces may be set as a function of the bit rate actually processed by the device.